



FT-817 Circuit Description

The FT-817 internal assembly consists of the MAIN Unit, Control (PANEL) Unit, and the PA Unit. The MAIN Unit contains the receiver front end, PLL IC, and switching circuits, and the VCO Unit for local signal Oscillation for transmission and reception. The PANEL Unit contains the CPU and reset circuit as well as the power circuitry for the LCD.

Receive Signal Circuitry

High-Frequency Circuit

The receive signal enters from ANT connector FRONT (J0001) or REAR (J0002) , selected by relay RL3016 on the PA Unit.

Signals between 0.1 and 154 Hz received at the antenna terminal pass through an input low-pass filter composed of L3081, L3082, C3264 and C3265.

Received 430 MHz signals, after passing through a high-pass filter composed of L3071, L3076, C3245 and C3254 are passed through low-pass filter composed of L3028, L3032, L3035, C076, C3082, C3088, and C3093, and directional coupler to the UHF T/R switch circuit composed of diode switch D3004, D3035 (both HSU277). Then it is fed to MAIN Unit via J3002.

Received 145 MHz signals, after passing through a high-pass filter composed of L3071, L3075, L3079, C3234, C3245, C3252, and C3260 are passed through low-pass filter composed of L3027, L3031, L3034, C3075, C3081, and C3092 and directional coupler to the VHF T/R switch circuit, composed of diode switch D3003, D3005 (both HSU277) . Then it is fed to MAIN Unit via J3002.

Received 0.1-54MHz signals, after passing through the first low-pass filter, are passed through low-pass filter composed of L3069, L3070, L3074, L3077, C3239, C3242, and C3248, and LPF 1-7 (5th or 7th-order Chebyscheff type filter),HPF 1-7, utilizing seven different sections for the various amateur bands at 0.1-54MHz, and 50MHz pre-amplifier (when combined) to the MAIN Unit via J3002.

The receive signal then passes through attenuator (−10dB when combined) which consists of resistors R1001, R1014, R1015, and diodes D1003, D1011 (both DAP236U) on the MAIN Unit.

Received 76-108MHz signal, after passing through a high-pass filter composed of L3071, L3075, L3079, C3234, C3245, C3252 and C3260 are passed through low-pass filter composed of L3027, L3031, L3034, C3075, C3081 and C3092, and directional coupler to the VHF T/R switch circuit, composed of diode switch D3003, D3005 (both HSU277). Then it is fed to MAIN Unit via J3002. The signal is fed to IC Q1025 (CXA1611N) which contains a front-end, and discriminator for WFM demodulation. Then the audio signal enters analog switch IC Q1049 (BU4066BF).

The FT-817 includes four receiver front ends, each optimized for a particular frequency range and mode combination.

1st Mixer Circuit/1st IF Circuit

The 1st mixer on the MAIN Unit consists of quad MOS FET D1047 (GN2011). The 1st local signal (68.430-538.330MHz) from the PLL Unit is applied to the gates of each FET in the 1st mixer.

The resulting output signal (the difference between the local signal and receive signal) passes through monolithic crystal filter (MCF) XF1001 (MF68R, BW: $\pm 7.5\text{kHz}$) to obtain the 1st IF signal having a center frequency of 68.33MHz. The signal is fed to the 2nd mixer circuit on the MAIN Unit after it is amplified by FET Q1051 (BB304C).

2nd Mixer Circuit/2nd IF Circuit

The 2nd mixer consists of FETs Q1060 and Q1062 (both 2SK302Y) on the MAIN Unit. The 2nd local signal (67.875MHz) is amplified by Q1047 (2SC4154E) and is applied to each FET's gate in the 2nd mixer.

The signal output from the ~~3rd~~ 2nd mixer passes through a ceramic filter, or optional mechanical filter (U1003), to become the 455-kHz 3rd IF signal.

Noise Blanker Circuit

A sample of the 2nd IF circuit is amplified by FETs Q1052 and Q1061 (both BB301C) on the MAIN Unit, and then rectified by D1068(1SS372). This output passes through R1343 and R1345, C1360 and C1362, and Q1076 (2SC4154E) to yield an average AGC voltage for controlling the amplification gain of the above FETs. Noise pulses contained in the output from D1075 are detected by Q1074 (2SC4154E) and are used to control the NB Gate.

AGC Circuit

The AGC circuit consists of D1064 (1SS372), transistor Q1066 (2SC4154E), etc. on the MAIN Unit. Output from the AGC circuit is fed back to the RF AGC circuit that consists of FETs of the IF amplifier stages, by which the output is controlled.

FM IF Circuit/FM Demodulator Circuit

The 2nd IF signal is fed to IC Q1069 (BA4116FV) for FM demodulation.

The FM demodulator IC contains a mixer, limiter amplifier, filter amplifier, squelch trigger, and demodulator. The IF input signal is band-limited by ceramic filter CD1002 (CDBC455CX24, BW: $\pm 4\text{kHz}$), amplified by the limiter amplifier, and demodulated into an audio signal by the demodulator. It then passes through a filter (R1308 and C1293). The signal passes through a de-emphasis circuit, which consists of R1256 and C1286.

The squelch circuit selectively amplifies the noise component of the demodulator output by the filter amplifier inside the FM IC and the active band-pass filter consisting of an externally attached resistor and capacitor. This circuit uses a signal detected by D1065 (DA221).

SSB/CW Demodulator Circuit

The 2nd IF signal is applied to the SSB demodulator Q1055 (SN16913) on the MAIN Unit, which produces audio by applying the carrier signal from the CAR-DDS IC (Q1031). Similarly, the CW signal is demodulated by a carrier signal, which is offset by the "Pitch" frequency.

The demodulated SSB and CW signals are each stripped of high-frequency components by an active low-pass filter which consists of op-amp IC Q1093-1 (NJM2902V). Then, they enter the VR Unit via J1008 through the PANEL Unit.

AM Demodulator Circuit

The 2nd IF signal from the IF Unit is applied to diode D1060 (BAS316) for AM demodulation.

The output from the detector passes through analog switch Q1049 (BU4066BF). Then, it enters the VR Unit via J1008 through the PANEL Unit.

Low-Frequency Amplifier Circuit

The demodulated signal that is selected by one of analog switches IC Q1057 (according to

the reception mode) passes through the low-frequency amplifier IC Q1094 (NJM2902V) , volume VR4901, and IC Q1070 (TDA7233D) for low-frequency power to drive the internal or external speaker with a maximum output of approximately 1.0W.

Transmit Signal Circuitry

Microphone Amplifier Circuit

The audio signal from microphone jack J1014 on the MAIN Unit is amplified by transistor Q1092 (2SC4154E) on the MAIN Unit, and then is applied to electronic volume IC Q1071 (M62364EP), which is controlled by User Menu operation.

The output (audio signal) from the electronic volume IC is amplified by Q1096 (NJM2902V) and fed to balanced modulator IC Q1087 (SN16913) through the low-pass filter IC Q1096 (NJM2902V).

During FM transmission, the audio signal is adjusted by software User Menu operation (Item # 29: FM_MIC). The audio signal that has passed through the pre-emphasis circuit which consists of C2201 and R2228 on the MAIN Unit is mixed with a tone signal from CPU IC Q4004, and is amplified and limited by op-amp IC Q1095-4 (NJM2902V) of the IDC circuit. The audio then passes through the splatter filter (secondary active low-pass filter) formed by op-amp IC Q1095-1 (NJM2902V), R1321, and R1322, plus C1344, and is then fed to the frequency-modulator circuit on the MAIN Unit through R1183 and R1477 for setting of the frequency deviation.

SSB Modulator Circuit

The carrier signal appropriate to the transmitting mode (LSB or USB) is applied from the CAR-DDS Unit to balanced modulator IC Q1087 (SN16913) on the MAIN Unit, and is modulated by microphone audio.

The balanced modulator produces the upper and lower side bands and carrier signal. The carrier and audio signal are suppressed and the carrier balance is adjusted by VR1001. As a result, the output signal obtained is a DSB signal with a carrier suppression of 30 dB or more.

The DSB modulated signal (1st IF signal: 455 kHz) then passes through ceramic filter CF1004 (CFJ455K14) or optional mechanical filter U1003 on the MAIN Unit, stripping residual carrier and the undesired sideband; the signal then passes as an SSB signal

through buffer-amplifier Q1040 (BB301C).

AM Modulator Circuit

As in the SSB modulator circuit, a carrier signal appropriate to the transmitting mode (AM) from the CAR-DDS Unit and an audio signal from the microphone are applied to balanced modulator IC Q1087 (SN16913) on the MAIN Unit.

The control signal from MODE SW IC Q1021 (BU4094BCFV) on the MAIN Unit causes a voltage of AM 5V to be sent from transistor Q1079 (2SC4154E). This voltage is applied to IC Q1087 via D1077 (BAS316), causing the balanced modulator to lose balance. The restored carrier signal and modulated signal are then fed to the TX mixer via ceramic filter CF1004 (CFJ455K14) on the MAIN Unit.

Frequency Modulation Circuit

The FM circuit uses a voltage controlled crystal oscillator (VCXO) which consists mainly of Q1033 (2SC4400), X1001 on the MAIN-Unit, varactor diode D1056 (HVC362), and T1018. The VCXO has a center frequency of 22.7785MHz.

The FM signal is produced by applying a signal from the FM microphone amplifier circuit to varactor diode D1056 and varying the crystal oscillator load capacity in proportion to the signal voltage.

CW (A1) Signal Generator Circuit

When the transmitting mode is CW (A1), the control signal from D-A converter IC Q1077 (M62353GP) on the MAIN Unit causes a CW 5V voltage. The voltage is applied to balanced modulator IC Q1087 via D1071, providing a carrier from the balanced modulator for the input to the transmit signal circuit of the MAIN Unit.

1st IF Circuit/1st Mixer Circuit

The 455 kHz 1st IF signal from the modulator circuit is band-limited by the MAIN Unit's ceramic or optional mechanical filter CF1004, U1003 (XF5201 or XF5301) according to the selected mode (CW, SSB, or AM). It is then buffer-amplified by FET Q1040 (BB301C) and fed to 1st mixer IC Q1038 (SN16913).

The IF Unit's double balanced mixer IC Q1038 (DBM) is used as the 1st mixer. A local signal (67.875MHz) is tripled REF frequency by Q1047 (2SC4154E) and fed to the local port of

DBM IC is mixed with the 455 kHz 1st IF signal to produce a 68.33MHz 2nd IF signal.

2nd IF Circuit/2nd Mixer Circuit

The 2nd IF signal passes through the crystal filter XF1001 whichever is appropriate to the selected mode (CW, SSB, or AM). It is fed to the 2nd mixer circuit.

The 2nd mixer consists of the MAIN Unit's D1049 (HSB88WS). The 2nd local signal (68.430-538.330MHz) from the PLL Unit is applied to the gates of each FET in the 2nd mixer.

High-Frequency Transmit Preamplifier Circuit

The transmit signal is passed through a low-pass filter (1.8-29.7MHz), a high-pass filter (50-54MHz), a band-pass filter (144-146MHz), a band-pass filter (430-440MHz) which consist of various inductors, and various capacitors, is amplified by Q1001 (UPC2710), and is passed onward to the PA Unit via J1002.

Power Amplifier Circuit

The transmit signal from the MAIN Unit arrives at connector J3001 on the PA Unit.

The transmit signal (1.8 MHz to 430 MHz) delivered to the PA Unit is amplified by pre-driver Q3001 (2SC3357), driver Q3002 (2SK5296) and final amplifiers Q5401/Q5402 (2SK2975).

Low-Pass Filter (LPF) Circuit

The transmission signal from the power amplifier circuit is passed through a low-pass filter, which consist mainly of RL3001-RL3015, RL3017, various inductors, and various capacitors. The LPF is a 5th or 7th-order Chebyshev type filter, utilizing nine different sections for the various amateur bands at 1.8 ~ 430MHz.

The low-pass filtered transmission signal is fed to the FRONT ANT connector (J0001) or REAR ANT connector (J0002) through the triplexer and directional coupler.

The directional coupler samples a part of the transmission power to detect forward power and reflected power. A DC voltage corresponding to the relative forward/reflected power is produced by D3032, D3033 (both MA716, 1.8 to 54MHz), D3009 D3017 (both MA716, 144 to 148MHz), D3007, D3008 (both MA716, 430 to 450MHz) , and is used for automatic level control (ALC).

ALC Circuit

The output from the directional coupler is routed from connector J3004 and applied to the ALC circuit via connector J1003 on the MAIN Unit.

The ALC circuit consists of an op-amplifier circuit for amplifying the forward and reflected voltage, a time-constant ALC amplifier, and a transmit signal control circuit on the MAIN Unit.

The forward voltage from connector J1003 on the MAIN Unit is added with a DC control voltage and is then applied to op-amp IC Q1097 (NJM2902V).

The reflected voltage is added with a DC control voltage and is then applied to op-amp IC Q1098 (NJM2904V). In the high SWR conditions (SWR 3:1 or more), transmitter output is reduced and a "High SWR" warning appears, thus protecting the PA Unit for potential damage.

The ALC amplifier amplifies the forward wave output via transistor Q1019 (2SC4154). This output then passes through a fast-attack, slow-delay RC time-constant circuit, which consists of R1097 and C1113 for the input to the TX signal control circuit on the MAIN Unit.

The TX control circuit adjusts the IF amplifier gain via gate 2 of FET Q1007 (BB304C) of the 68.33 MHz IF amplifier circuit to prevent the TX output from exceeding the preset level.

PLL Frequency Synthesizer

The PLL Frequency Synthesizer consists mainly of a master reference oscillator circuit, 2nd local oscillator circuit, PLL IC, CAR-DDS, REF-DDS units which digitally synthesize carrier outputs, and a PLL circuit which contains a voltage controlled oscillator (VCO).

Master Reference Oscillator Circuit

The master reference oscillator uses a X'tal Oscillator (oscillation frequency: 22.625MHz) composed of Q5001 (2SC4400-4), X5001, TC5001, C5001, R5005, etc.

The reference oscillator signal passes through a buffer amplifier Q5002 (2SC4400-4), C5004, C5007, R5003, R5004, R5007.

It is then fed to the MAIN Unit via J5002.

CAR-DDS Circuit /REF-DDS Circuit

DDS ICs Q1031 (AD9835BRU), and Q2016 (AD9850BAS) each contain a shift register, selector, phase accumulator, and ROM.

The reference oscillation frequency (22.625MHz) that is delivered to each of the DDS Units is applied to each DDS IC after amplification by transistors Q1028/Q2020 (both 2SC4400-4).

The DDS outputs contain digital amplitude data corresponding to serial frequency data from CPU IC Q4004 of the PANEL Unit. The DDS frequency range is 453.5 ~ 466.5kHz (cf = 455.0 kHz) for the CAR-DDS, 7.2-8.0MHz for the REF DDS.

2nd Local Oscillator Circuit

The 2nd LO circuit is a Hartley-type overtone oscillator circuit (frequency: 67.875MHz) composed of Q1047 (2SC4400) on the MAIN Unit.

1st Local Oscillator Circuit

VCO output is buffer-amplified by Q2008 (2SC4400), Q2011, Q2014, Q2016 (both 2SC5374) and passes through a LPF. It is then fed to the TX/RX frequency mixer circuitry of the MAIN Unit.

PLL Circuit

The PLL circuit is a frequency mixing type composed of a VCO, mixer, PLL IC, and loop filter.

The VCO consists of five circuits (VCO1, VCO2, VCO3, VCO4 and VCO5), with a frequency range of 68.430-538.330 MHz divided into five bands, allocated to the five VCO circuits. VCO1-VCO5 consist mainly of FETs Q2004, Q2005, Q2006 (all 2SK210GR), transistors Q2009, Q2010 (both 2SC5374), and diodes, D2001-D2006 (all HVC362), D2007 (1SV282), D2008 (1SV281), D2009 (1SV286) and coils T2001-T2003, L2010, L2011.

The VCO switching signal from the connector J2002 is used to drive switching transistors Q2001, Q2002, Q2003, Q2012, Q2013 (all DTC124EU) to switch the source terminal of the oscillator FET.

The 68.430-538.330 MHz VCO signal is fed to mixer D1047 (GN2011-Q).

The REF-DDS signal (7.2-8.0MHz) is fed to PLL IC Q2022 (FQ7925) after it passes through a LPF composed of C2064, C2067, C2069, C2071, C2075, L2014, L2015, and L2016, and buffer amplifier Q2019 (2SC4400-4).

The phase of the reference frequency and that of the signal input to PLL IC are compared, and a signal whose pulse corresponds to the phase difference is produced. The VCO frequency is controlled by a first lag filter which consists of R2057, R2065, R2062, and C2090 and a secondary lag filter composed of C2085, C2088, and R2053.

Control Circuitry

Microprocessor Circuit

The microprocessor circuit, which is composed of CPU IC Q4004 (HD64F2345) and EEPROM IC Q4004 (ATC64N-10S1), performs various types of processing, such as control signals, serial I/O, A/D conversion, dial counter circuit control, key input, and display functions.

The EEPROM memorizes various parameters and settings (transmission frequency range, transmission output control) and carrier points according to the transceiver version and the contents of memory channels.

Reset Circuit

The reset circuit consists mainly of PANEL Unit ICs Q4014 (PST3445), Q4015 (2SC4154E), Q4011 (2SA1602A), Q4016 (2SC4154E), and Q4010 (2SA1602A), capacitors, and resistors. This circuit controls the power-down input port, CPU reset input, keyer CPU, and related circuits.

Dial Counter Circuit

The dial counter circuit consists of Main Dial and SEL Knob. This circuit detects a two-phase pulse having a phase difference of 90 degrees and delivers it to CPU IC Q4006.

Serial Data Communication Circuit

The Serial Data Communication Circuit consists of ICs Q4008, Q4009, Q4010 etc. on the PANEL-unit. These ICs distributes a pair of serial data (Data/Clock/Strobe) generated by CPU to the various devices, such as CAR-DDS, REF-DDS, E.VOL, D/A or Shift-Resistor for controlling analog switching, band switching, VCO selection, and so on.

Serial data communication is performed by a clock synchronous for the above purposes, whereas the serial data is transferred to the asynchronous signal for the CAT system.

Various types of data, such as operating frequency, mode, and display data, are processed by CPU IC Q4004.

The CAT (external computer control) signals are converted to RS232 interface standard levels by Option CAT Interface Cable (CT-62).

Key Matrix Circuit

The key matrix circuit consists of PANEL Unit D4001-D4003.D4006 (all IMN10) and the panel key switches arranged on the matrix. When a key is pressed, this circuit reads the input data for processing by the CPU.

Analog-Digital Converter Circuitry

Forward and reflected-wave voltage, ALC, DISC, S-meter, etc. are selected by MAIN Unit IC Q1073 (BU4053BCF) and are fed to the A/D port of CPU IC Q4004 for conversion into digital values to be processed.

The individual voltages, converted into digital values, are displayed as PO, SWR, ALC, VCC, and S-meter indications on the LCD panel.

LED Drive Circuit

The LED drive circuit consists of PANEL Unit TRs Q4018 and Q4019 (both 2SC1623) and the LEDs. This circuitry drives (turns on/off) the appropriate LEDs.

LCD Circuit

Data processed by the CPU IC is sent as parallel data to LCD Unit DS4001 .

CTCSS Tone Generator Circuit

The CTCSS tone generator circuit consists mainly of CPU IC Q4004 and active filter IC Q1094 (NJM2902).

Electronic Keyer Circuit

The electronic keyer circuit consists of CPU IC Q4004. When the CW mode is selected, this circuit controls the generation of Morse characters.